



THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Atty. Docket:

TSE-HUA LAN ET AL

US010341

Serial No.: 09/912,132

Group Art Unit: 2613

Filed: July 24, 2001

Examiner: C. Parsons

Title: REDUCED COMPLEXITY VIDEO DECODING AT FULL
RESOLUTION USING VIDEO EMBEDDED RESIZING

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313-1450

Commissioner for Patents
BOX APPEAL BRIEF - PATENTS
Alexandria, VA 22313-1450

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Technology Center 2600

Sir:

Enclosed is an original plus two copies of an Appeal

Brief in the above-identified patent application.

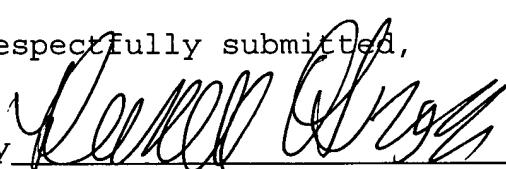
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No. 14-1270.

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Respectfully submitted,

By 
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APPEAL BRIEF

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Sir:

The rejection of Claims 1-12 is being appealed, which
are reproduced in the attached Appendix.

1. Real Party in Interest

The real party in interest is Koninklijke Philips
Electronics N.V., the assignee herein.

2. Related Appeals and Interferences

The Appellant is not aware of any appeals or
interferences that relate to the present application.

3. Status of all Claims

Claims 1-12 were submitted in the original application as filed. Claims 1-12 were finally rejected in the Office Action dated August 26, 2003.

4. Status of Amendment

No Amendments were filed subsequent to the Final Rejection of August 26, 2003.

5. Summary of the Invention

The present invention is directed to a method for decoding a video bitstream at a first resolution. As can be seen from Figures 2-3, the method includes residual error frames being produced at a second lower resolution, as described on pages 4 and 7. Motion compensated frames are also produced at the second lower resolution, as described on pages 5 and 7. As further described on pages 5 and 7, the residual error frames are combined with the motion compensated frames to produce video frame and up-scaled to the first resolution.

6. Issues Presented for Review

The issue on review is whether Claims 1-6 and 10-12 under 35 USC 103 are unpatentable over Choi (U.S. Patent No. 6,442,201) in view of Campisano et al. (U.S. Patent No. 6,470,051). The second issue is whether Claims 7-9 under 35 USC 103 as are unpatentable over Choi in view of Campisano et al., and in further view of Vetro et al. (U.S. Patent No. 6,519,288).

7. Grouping of the Claims

The Appellant respectfully submits Claims 1-12 either stand or fall together.

8. Arguments

Claims 1-6 and 10-12 stand finally under 35 USC 103 as being unpatentable over Choi (U.S. Patent No. 6,442,201) in view of Campisano et al. (U.S. Patent No. 6,470,051). Claims 7-9 stand rejected under 35 USC 103 as being unpatentable over Choi in view of Campisano et al., and in further view of Vetro et al. (U.S. Patent No. 6,519,288).

First of all, it is respectfully submitted that the proper motivation does not exist to combine Choi with Campisano et al.

On page 2100-124 of the MPEP, it is stated that if a proposed modification would render the prior art invention unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

In re Gordon, 733 F.2d 900, 221, USPQ 1125 (Fed. Cir. 1984).

In Choi, a down conversion decoding device is disclosed that is used to convert a HD signal to a lower resolution signal so that it may be displayed on an NTSC type analog television. This is made quite evident by the "Discussion of Related Art" section in Column 1, of Choi. Further, in column 10, lines 31-33, Choi discloses that the signal input for decoding is 1920x1080 and the display format is 852x480.

As described above, Choi discloses a down conversion decoding device that is used to convert a HD signal to a lower resolution signal so that it may be displayed on an NTSC type analog television. In the present rejections, Choi is being modified to include the up-sampling of Campisano et al.

However, by making this modification, frames processed by such a combination could no longer be displayed on an NTSC type analog television. Thus, the modification

proposed in the present rejections does render Choi unsatisfactory for its intended purpose. Therefore, it is evident that the proper motivation does not exist to combine Choi with Campisano et al.

Further, it is respectfully submitted that the combination of Choi in view of Campisano et al. neither teaches nor suggests all of the claim limitations. In particular, such features include "producing residual error frames at a second lower resolution".

In addressing this feature in the above rejections, the 4x8 IDCT unit shown in Figure 5 of Choi is being relied on. However, in reviewing Choi nowhere is it disclosed that 4x8 IDCT unit produces residual error frames at a second lower resolution.

As can be seen from Figure 5 of Choi, a decimation unit is placed only after the adder 59. Since the adder 59 combines the outputs of the 4x8 IDCT unit 54 and the motion compensation unit 58, this implies that only the output frames of Choi are produced at a lower resolution. In view of this, Choi cannot be reasonably interpreted as disclosing "producing residual error frames at a second lower resolution", as required by the claims. Therefore,

it is respectfully submitted that this feature is distinguishable over Choi in view of Campisano et al.

In view of the above-described distinctions, it is respectfully submitted that the invention of Claims 1-12 is not made obvious by Choi in view of Campisano et al . alone or in combination with Vetro et al. Therefore, the Appellant respectfully requests that the final rejection of these claims be reconsidered and reversed.

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Respectfully submitted,

By 
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By Elissa De Luccy
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A P P E N D I X

1. A method for decoding a video bitstream at a first resolution, comprising the steps of:

producing residual error frames at a second lower resolution;

producing motion compensated frames at the second lower resolution;

combining the residual error frames with the motion compensated frames to produce video frames; and

up-scaling the video frames to the first resolution.

2. The method of claim 1, wherein the producing residual error frames includes performing an 8X8 inverse discrete transform to produce pixel values.

3. The method of claim 2, wherein the pixel values are sampled at a predetermined rate.

4. The method of claim 1, wherein the producing residual error frames includes performing a 4X4 inverse discrete transform.

5. The method of claim 1, wherein the producing motion compensated frames includes scaling down motion vectors by a predetermined factor to produce scaled motion vectors.
6. The method of claim 5, wherein motion compensation is performed based on the scaled motion vectors.
7. The method of claim 1, wherein the up-scaling is performed by a technique selected from a group consisting of repeating pixel values and linear interpolation.
8. The method of claim 1, wherein the up-scaling is performed in a horizontal direction.
9. The method of claim 1, wherein the up-scaling is performed in a same direction as down scaling in the residual error frames.
10. A memory medium including code for decoding a video bitstream at a first resolution, the code comprising:
 - a code for producing residual error frames at a second lower resolution;

a code for producing motion compensated frames at the second lower resolution;

a code for combining the residual error frames with the motion compensated frames to produce video frames; and

a code for up-scaling the video frames to the first resolution.

11. An apparatus for decoding a video bitstream at a first resolution, comprising:

means for producing residual error frames at a second lower resolution;

means for producing motion compensated frames at the second lower resolution;

means for combining the residual error frames with the motion compensated frames to produce video frames; and

means for up-scaling the video frames to the first resolution.

12. An apparatus for decoding a video bitstream at a first resolution, comprising:

a first path producing residual error frames at a second lower resolution;

a second path producing motion compensated frames at the second lower resolution;

an adder combining the residual error frames with the motion compensated frames to produce video frames; and

an up-scaler increasing the video frames from the second resolution to the first resolution.